PATENT
8733.527.00

IN THE UNITED STATES PATENT APPLICATION

OF

JONG JIN PARK
KU HYUN PARK
AND
HYEON HO SON

FOR

LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

LONG ALDRIDGE & NORMAN, LLP
701 Pennsylvania Avenue, N.W.
Sixth Floor, Suite 600
Washington, D.C. 20004
Telephone No.: (202) 624-1200
Facsimile No.: (202) 624-1298

[0001] This application claims the benefit of Korean Patent Application No. P2000-85272 filed December 29, 2000, which is hereby incorporated by reference, as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates to a liquid crystal display and a driving method thereof, and more particularly to a liquid crystal display and a driving method thereof for improving a picture quality.

Description of the Related Art

[0003] Generally, an active matrix liquid crystal display device controls the light transmissivity of liquid crystal by the electric field applied to the liquid crystal, for displaying a picture. For this, the liquid crystal display device, as shown in Fig. 1, includes a liquid crystal display panel 2 in which a plurality of liquid crystal cells are arranged in a matrix between two transparent substrates, a gate driver 6 connected to a plurality of gate lines (GL1 to GLm) of the liquid crystal display panel 2, and a data driver 4 connected to a plurality of data lines (DL1 to DLn) of the liquid crystal display panel 2.

[0004] The gate driver 6 sequentially supplies scanning signals to m gate lines (GL1 to GLm) and drives a thin film transistor TFT connected to the corresponding gate lines (GL1 to GLm). The data driver 4 is synchronized with the scanning signals being sequentially supplied to the gate lines (GL1 to GLm) and supplies the data corresponding to a brightness value of video data to the data lines (Dl1 to DLn). In other words, the conventional liquid

crystal display sequentially turns on/off for a frame period the whole gate lines (GL1 to GLm) formed in the liquid crystal panel 2 and supplies to the data lines (DL1 to DLn) the corresponding data to the gate lines (GL1 to GLm) for displaying the picture.

[0005] Fig. 2 is a diagram representing in detail a conventional gate driver.

[0006] Referring to Fig. 2, the conventional gate driver 6 includes a shift register 8 for receiving scan data from a supplier 14 and for shifting the supplied scan data, a level shifter 10 for receiving the scan data from the shift register 8 and for shifting a voltage level suitable for driving the liquid crystal display panel 2, and an outputter for receiving data from the level shifter 10 and for supplying to the liquid crystal display panel 2.

[0007] The supplier 14 supplies the scan data corresponding to '1' to a first bit of the shift register 8. The shift register 8 supplies the scan data corresponding to '1' supplied to a first bit in response to a clock signal (XGA, for example) (not shown), to a first bit of the level shifter 10 and a second bit of itself. The supplier 14 does not supply to the shift register 8 the scan data corresponding to '1' until the scan data corresponding to '1' is shifted to a m^{th} bit of the shift register 8. In other words, there is only one scan data corresponding to '1' in the shift register 8.

[0008] Meanwhile, the shift register 8 sequentially moves to the m bit the scan data of '1' supplied to the first bit of itself, and supplies the scan data to each bit of the level shifter 10. When the scan data of '1' is supplied from the shift register 8, the level shifter 10 outputs a gate high volt (Ghv) to the outputter 12 by shifting the voltage level (around 20V). Also, when the scan data of '0' is supplied from the shift register 8, the level shifter 10 outputs a gate low volt (Glv) to the outputter 12 by shifting the voltage level (around –5V).

[0009] The outputter 12 supplies the scan data applied from the level shifter 10 to the liquid crystal display panel 2. If the scan data of '1' is currently supplied to a m-10^{th} gate

line (GLm-10), the liquid crystal display panel 2 is divided into the picture of a current frame 16 and the picture of a previous frame 18 on the basis of the m-10th gate line (GLm-10) as shown in Fig. 3.

[0010] Accordingly, if a moving picture which moves from right to left, is displayed in the liquid crystal display panel 2, the moving picture 20 displayed in the current frame 16 and the moving picture (22) displayed in the previous frame 18 appear to be crossing each other on the basis of the m-10th gate line (GLm-10) as shown in Fig. 4A. At this moment, the picture of the current frame and the picture of the previous frame overlap each other as much as the part 24 by which the moving picture 20 displayed in the current frame 16 moves, as shown in Fig. 4B. Thereby, a motion blur phenomenon occurs, resulting in the deterioration of the picture quality of the liquid crystal display panel 2.

[0011] In the meantime, a plurality of pixels on the liquid crystal panel 2 can be represented as an equivalent circuit shown in Fig. 5. In Fig. 5, a pixel includes a TFT connected with a gate line (GL), a data line (DL) and a common voltage line (CL), and a liquid crystal cell (Clc) connected with a drain terminal of the TFT and the reference voltage line (CL). Also, the pixel includes a parasitic capacitor (Cgs) formed between the drain terminal of the TFT and the gate line (GL), and a storage capacitor (Cst) between the parasitic capacitor (Cgs) and a ground voltage source (GND).

[0012] A data pulse is supplied to the data line (DL) when the gate high volt (Ghv) is supplied to the gate line (GL) of the liquid crystal display panel 2 as shown in Fig. 6. The voltage of the data pulse drops as much as the changed voltage (ΔVp) when the gate high volt (Ghv) is changed to a low state. As a result, the deterioration of the brightness of the liquid crystal display panel 2, that is, the deterioration of the picture quality of the liquid crystal

display panel 2, occurs. The voltage drop amount (ΔVp) of the data pulse is determined by the following equation 1.

EQUATION 1 $$\Delta V_P = C_{gs}/C_{gs}+C_{st}+Clc(V_{gh}-V_{gl.})$$

(wherein Clc is a capacitor of a liquid crystal cell, Vgh represents a voltage value of a gate high volt and Vgl represents a voltage value of a gate low volt.)

[0013] In the equation 1, a parasitic capacitor (Cgs), a storage capacitor (Cst), a voltage value of the gate high volt and a voltage value of the gate low volt are fixed, and the capacitor value of the liquid crystal cell (Clc) is determined by the picture displayed. If a still picture is displayed in the liquid crystal display panel 2, the capacitor value of the liquid crystal cell (Clc) can be predicted in advance. Accordingly, the voltage drop amount (ΔVp) of the data pulse can also be predicted so that the voltage drop amount (ΔVp) of the data pulse can be compensated.

[0014] However, if the moving picture is displayed in the liquid crystal display panel 2, the capacitor value of the liquid crystal cell (Clc) cannot be predicted in advance. Accordingly, the voltage drop amount (ΔVp) of the data pulse cannot be predicted. Accordingly, the voltage drop amount (ΔVp) of the data pulse is not compensated, thus the picture quality of the liquid crystal display panel 2 is deteriorated.

SUMMARY OF THE INVENTION

[0015] Accordingly, the present invention is directed to a liquid crystal display and driving method thereof that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0016] Accordingly, it is an advantage of the present invention to provide a liquid crystal display and a driving method thereof for improving a picture quality.

[0017] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. Other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof, as well as the appended drawings.

[0018] In order to achieve these and other advantages of the invention, a method of driving a liquid crystal display according to one aspect of the present invention includes the steps of supplying a first scanning signal to a first gate line positioned at a specific location among a plurality of gate lines for driving a liquid crystal cell; supplying a second scanning signal to a second gate line which is formed while having at least one gate line between said first gate line and said second gate line after said first gate line scanning signal has been supplied; and supplying the data synchronized with said first scanning signal and said second scanning signal to a plurality of data lines formed in the manner of crossing with the plurality of said gate lines.

[0019] In the method, said first scanning signal and said second scanning signal are sequentially supplied to the plurality of said gate lines.

[0020] The method further includes supplying picture data to the plurality of said data lines in synchronization with said first scanning signal; and supplying black data to the plurality of said data lines in synchronization with said second scanning signal.

[0021] The method further includes supplying picture data to the plurality of said data lines in synchronization with said second scanning signal; and supplying black data to the plurality of said data lines in synchronization with said first scanning signal.

[0022] A liquid crystal display according to another aspect of the present invention includes a liquid crystal display panel where a plurality of liquid crystal cells are arranged in a matrix type; a plurality of gate lines formed in said liquid crystal panel; a plurality of data lines formed in a manner of crossing with the plurality of said gate lines; a gate driver supplying a first scanning signal and a second scanning signal to the plurality of said gate lines; a scanning signal supplier supplying said first scanning signal and said second scanning signal to said gate driver; and a data driver supplying to the plurality of said data lines the data synchronized with said first scanning signal and said second scanning signal.

[0023] In the liquid crystal display, said first scanning signal and said second scanning signal are alternately and sequentially supplied.

[0024] In the liquid crystal display, said data driver supplies black data to said data line when said first scanning signal is supplied to one of said gate lines, and picture data is supplied when said second scanning signal is supplied to a gate line which is formed as having at least one gate line between itself and the gate line to which said first scanning signal is supplied.

[0025] In the liquid crystal display, said gate driver includes a first shift register sequentially for receiving said first scanning signal and said second scanning signal from said scanning signal supplier; a second shift register for receiving into an i (i is a natural number) bit of itself the data stored at the i bit of said first shift register and transmitting to i+1 bit of said first shift register the data stored at the i bit of itself; a level shifter for receiving the data that contain any one of said first scanning signal and said second scanning signal from said first shift register, and changing a voltage level suitable for driving said liquid crystal display panel; and an outputter for receiving from said level shifter the data of which the voltage level has been changed and for supplying to said liquid crystal display panel.

[0026] In the liquid crystal display, said scanning signal supplier supplies said second scanning signal to said first shift register when said first scanning signal is positioned at said second shift register.

[0027] In the liquid crystal display, said gate driver includes a first shift register sequentially receiving said first scanning signal and said second scanning signal from said scanning signal supplier; a second shift register receiving into an i (i is a natural number) bit of itself the data stored at the i bit of said first shift register and transmitting to i+1 bit of said first shift register the data stored at the i bit of itself; a level shifter receiving the data that contain any one of said first scanning signal and said second scanning signal from said second shift register, and changing a voltage level suitable for driving said liquid crystal display panel; and an outputter receiving from said level shifter the data of which the voltage level has been changed and supplying to said liquid crystal display panel.

[0028] In the liquid crystal display, said scanning signal supplier supplies said second scanning signal to said first shift register when said first scanning signal is positioned at said second shift register.

[0029] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0031] In the drawings:

[0032] Fig. 1 schematically illustrates a conventional liquid crystal display device;

[0033] Fig. 2 illustrates a gate driver shown in Fig. 1;

[0034] Fig. 3 represents a process of displaying a picture in the liquid crystal display panel shown in Fig. 1;

[0035] Figs. 4A to 4B represent a process of displaying a moving picture in the liquid crystal display panel shown in Fig. 1;

[0036] Fig. 5 is an equivalent circuit diagram of the liquid crystal display panel shown in Fig. 1;

[0037] Fig. 6 represents a data pulse applied to a liquid crystal cell shown in Fig. 5;

[0038] Fig. 7 illustrates a gate driver according to an embodiment of the present invention;

[0039] Fig. 8 is a waveform diagram representing a motion process of a data driver and a gate driver of the present invention;

[0040] Figs. 9 and 10 represent the process of displaying a picture in the liquid crystal display panel by the gate driver shown in Fig. 7;

[0041] Fig. 11 is a waveform diagram representing a motion process of a data driver and a gate driver according to another embodiment of the present invention; and

[0042] Fig. 12 particularly illustrates a gate driver according to still another embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

[0043] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0044] With reference to Figs. 7 to 12, embodiments of the present invention is explained as followings.

[0045] Fig. 7 particularly illustrates a gate driver according to an embodiment of the present invention.

[0046] Referring to Fig. 7, the gate driver according to the embodiment of the present invention includes a supplier 30 supplying scan data, a first shift register 32 receiving the scan data from the supplier 30, a second shift register 38 receiving the scan data from a i^{th} bit of the first shift register 32 and supplying the scan data to a $i+1^{st}$ bit of the first shift register 32, a level shifter 34 receiving the scan data from the first shift register 32 and shifting a voltage level suitable for driving the liquid crystal display panel, and an outputter 36 receiving data from the level shifter 34 and supplying to the liquid crystal display panel.

[0047] To describe in detail the motion process of the gate driver, firstly, supplier 30 supplies a scan data corresponding to '1' to a first bit of the first shift register 32. Then the first shift register 32 supplies the provided scan data to a first bit of the level shifter 34 and a first bit of the second shift register 38.

[0048] The level shifter 34 supplies a gate high volt (Ghv) stored at the first bit of the level shifter 34 and corresponding to the scan data of '1' to a first bit of the outputter 36. Also, the level shifter 34 supplies a gate low volt (Glv) stored at the second through the m^{th} bit of the level shifter 34 and corresponding to the scan data of '0' to the second through the m^{th} bit of the outputter 36. After that, the outputter 36 supplies the gate high volt (Ghv) and the gate low volt (Glv) to the liquid crystal display panel.

[0049] Meanwhile, the second shift register 38 transmits to the second bit of the first shift register 32 the scan data supplied to the first bit of the second shift register 38. While having these processes repeated, the gate driver sequentially scans a plurality of gate lines

(GL1 to GLm). In the meantime, the supplier 30 supplies the scan data of '1' to the first shift register 32 when the scan data of '1' is positioned at any bit of the second shift register 38.

[0050] For example, the supplier 30 supplies the scan data of '1' to the fist bit of the first shift register 32 when the scan data of '1' is positioned at a third bit of the second shift register 38. In this way, the gate high volt (Ghv) is supplied to the first gate line (GL1) when the scan data of '1' is supplied to the first bit of the first shift register 32.

[0051] After this, the scan data of '1' provided to the first bit of the first register 32 is transmitted to the first bit of the second register 38, and the scan data of '1' temporarily stored at the third bit of the second register 38 is transmitted to a fourth bit of the first register 32. Therefore, the gate high volt (Ghv) is supplied to a fourth gate line (GL4) after the gate high volt (Ghv) being supplied to the first gate line (GL1). In other words, two gate lines alternately receive the gate high volt (Ghv) in the present invention. For this, in the present invention, there is supplied to the gate driver the pulse signals (XGA, for example) having twice as high a frequency as in the conventional method.

[0052] Currently, if the scan data of '1' is alternately supplied to a m-10th the gate line (GLm-10) and a m-20th the gate line (GLm-20), as shown in Fig. 8, an actual data (D) and a reset data (R) are sequentially supplied to a plurality of data lines (DL) during 1 horizontal synchronization signal (Hsync). For this, in the present invention, there can be supplied to the data driver the pulse signals having twice as high a frequency as in the conventional way. The actual data (D) and the reset data (R) can be sequentially supplied because the data driver of the present invention additionally functions to output the reset data (R).

[0053] A black screen is displayed between the m-10th gate line (GLm-10) and the m-20th gate line (GLm-20) in the liquid crystal display panel 44, as shown in Fig. 9, when the data driver and the gate driver are driven as shown in Fig. 8. In other words, when the scan data of '1' is supplied to the m-20th gate line (GLm-20), the actual data (D) to be displayed in the liquid crystal display panel 44 is supplied from the data driver. Also, the data driver supplies a black data, that is, the reset data (R), when the scan data of '1' is supplied to the m-10th gate line (GLm-10).

[0054] Accordingly, the picture to be displayed is displayed on top of the black picture in the liquid crystal display panel 44 as shown in Fig. 10. In other words, the picture to be displayed currently is displayed on top of the picture displayed previously in conventional method, but is always displayed on top of the black picture regardless of the previous picture in this invention. Thereby, there can be prevented the motion blurring phenomenon which occurs due to the overlap of the picture to be displayed currently and the picture displayed previously. Also, the value of the liquid crystal capacitor (Clc) of the equation 1 is always fixed in this invention. That is, because the picture to be displayed currently is always displayed on top of the black picture, the value of the liquid crystal capacitor (Clc) is always fixed to the value with which the black picture is displayed. Consequently, the voltage drop amount (ΔVp) can be predicted in advance so that the voltage drop amount (ΔVp) can be compensated.

[0055] Meanwhile, the reset data (R) is inputted when the m-10th gate line (GLm-10) being scanned and the actual data (D) is inputted when the m-20th gate line (GLm-20) being scanned in Fig. 8. But, as in Fig. 11, it is possible that the actual data (D) is inputted when the m-10th gate line (GLm-10) being scanned and the reset data (R) is inputted when the m-20th gate line (GLm-20) being scanned. In other words, the scan data of '1' inputted first

from the supplier 30 to the first shift register 32 has a picture data inputted, then the scan data of '1' inputted next from the supplier 30 to the first shift register 32 has a black data inputted. In the same manner, the scan data of '1' inputted first from the supplier 30 to the first shift register 32 has a black data inputted, then the scan data of '1' inputted next from the supplier 30 to the first shift register 32 has a picture data inputted.

[0056] Also, the scan data can be inputted from the supplier 30 to the second shift register (50), as shown in Fig. 12, in the present invention. At this time, the first shift register 32 and the second shift register (50) have the same bit.

[0057] As in the foregoing description, in the liquid crystal display and the driving method thereof according to the present invention, two gate lines are alternately scanned in one frame, and black data is supplied when the first gate line is scanned and the picture data is supplied when the second gate line is scanned. Consequently, since the desired picture is displayed on top of the black picture in this invention, the motion blurring phenomenon can be prevented. Besides, the capacitor value of the liquid crystal can be predicted since the desired picture is displayed on top of the black picture. That is, because the capacitor value of the liquid crystal is fixed, the voltage drop amount of the data pulse can be predicted, thereby the voltage drop amount of the data pulse can be compensated.

[0058] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.